# Adaptive Power Decoupling Control for Single-Phase Converter with Unbalanced DC-Split-Capacitor Circuit

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***Abstract*—This paper proposes an adaptive power decoupling control strategy for a single-phase rectifier with an unbalanced split-capacitor decoupling circuit. Since a capacitance mismatch estimator is integrated into the control strategy, the impact of capacitance mismatch is eliminated. Meanwhile, the capacitance mismatch estimator can provide an auxiliary online monitor for the health of split-capacitors. Moreover, the mechanism of capacitor voltages self-balance is explained. Finally, experiments are conducted to verify the effectiveness of the proposed method.**

***Index Terms*—Active power decoupling, adaptive control, dc-split-capacitor, single-phase converter, capacitance mismatch.**

## I. Introduction

THE twice ripple power inherently exists in single-phase power electronics systems [1], [2]. To eliminate its adverse effects, active power decoupling methods are usually used to divert second-order ripple power away from the DC sources or loads [3], [4].

Lots of power decoupling circuit topologies have been proposed. Various bidirectional circuits, such as buck circuit [5], boost circuit [6], buck-boost circuit [7], and H-bridge circuit [8] are taken as the decoupling cells to buffer twice ripple power generally. These basic decoupling cells work independently with the original converters, which make them easy to control. In addition, some power converters with power decoupling are proposed, in which the power decoupling cell shares switch with the original circuits [9]–[11]. Then the count of the semiconductor devices of the power converter is reduced. Furthermore, a novel power converter with power decoupling by sharing energy storage units with the original circuits is proposed in [12]. The power decoupling cell is a symmetrical half-bridge converter. It is called a DC split-capacitor decoupling circuit. Based on the DC split-capacitor decoupling circuit, a power converter with reduced current stress and components is presented by sharing both switches and energy storage units [13].

Because of the features of higher order and higher degree of coupling, the control of the DC split-capacitor decoupling circuit has attracted much attention. Many power decoupling control schemes have been proposed for the DC split-capacitor decoupling circuit. In [14] an open-loop power decoupling control scheme is proposed, where the references of capacitor voltages are computed in theory. However, the related control performance heavily depends on the actual parameters such as decoupling capacitance and filter inductance. Addressing this problem, several closed-loop power decoupling control schemes are developed [15]–[17]. In [15], a dual loop voltage control strategy is proposed, where one loop is responsible for the rectifier control, and the other is for the power decoupling. This frame-transformation-based power decoupling control method in [15] effectively buffers the twice grid frequency ripple. In addition, a general transformation based on integrator and root operation is proposed to generate the desired multi-frequency voltage references [16]. Then, the multi-frequency ripple power caused by non-ideal grids can be mitigated. Besides, a multi-proportional resonant (PR) controller is adopted for the ripple power control loop in [17], and it achieves the same effect of suppressing multi-frequency power ripple. The difference between [16] and [17] is the fundamental frequency of capacitor ripple voltages. The fundamental frequency of the former one is grid frequency, while the latter is the twice grid frequency.

In the above studies, it is assumed that the capacitance values of the two split capacitors are completely the same. Since the real capacitances may drift differently (within $\pm 10\%$) due to thermal heating and aging [18], the assumption before is unreasonable in practice. Unfortunately, this will lead to the capacitance mismatch of the split-capacitors and deteriorate the decoupling performance and the grid current quality [19]. The mismatch about split capacitors is considered in [19], [20]. And control methods with immunity to capacitance mismatch are proposed. However, the proposed controllers are only applicable to the case where the fundamental frequency of capacitor ripple voltages is twice the grid frequency. And the problem of capacitance mismatch when the fundamental

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frequency of the capacitor ripple voltages is the grid frequency has not been resolved so far. This is the gap this paper will fill.

To cope with the negative effects due to the capacitance mismatch, an adaptive controller for the DC split-capacitor decoupling circuit is proposed. The main contributions of this paper are summarized as follows:

1) The proposed adaptive controller realizes active power decoupling accurately. The required current reference is obtained by the adaptive controller in closed-loop, and then the DC ripple power forces to zero.
2) The proposed control scheme is robust to the DC split-capacitor mismatch. The ripple power caused by the capacitor mismatch can be eliminated by estimating the capacitance unequal factor and modifying duty cycles.
3) The capacitance unequal factor is obtained online and it can be used for split-capacitors health monitoring because the unequal factor can reflect the health condition differences between the two split capacitors.
4) The reason for capacitor voltage self-balancing is explained from the perspective of stability.

The rest of the paper is arranged as follows: Section II briefly explains the circuit of the single-phase rectifier with DC-split-capacitor. And the steady-state feasible solution of split-capacitor voltages is analyzed in this section. Section III presents the average model of the system and then designs the adaptive controller to achieve closed-loop power decoupling. And the self-balance of capacitor average voltages is analyzed in this section. Section IV covers detailed experimental results to validate the effectiveness of the proposed controller. Finally, concluding remarks are provided in Section V.

## II. Circuit Configuration and Analysis

### A. Circuit Configuration

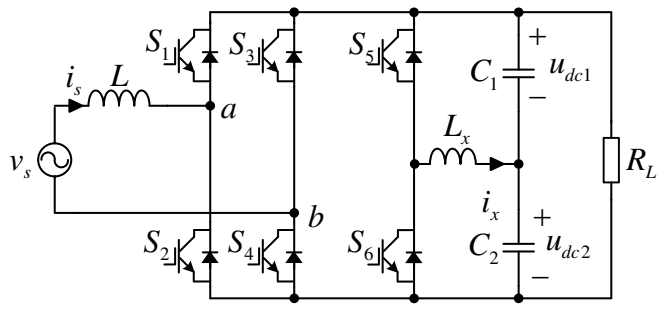


Fig. 1. The topology of the single-phase power converter with DC-split-capacitor power decoupling circuit.

The main circuit diagram of the single-phase AC/DC converter with DC-split-capacitor is shown in Fig. 1, which consists of a conventional full-bridge AC/DC rectifier, and a half-bridge ripple power decoupling circuit. The decoupling circuit is composed of a half-bridge, a small filtering inductor $L_x$, and a split-capacitor formed by two capacitors $C_1$ and $C_2$ in series. Two capacitors play dual roles in mitigating the inherent ripple power and filtering out the switching ripple. $L_x$ is used to connect the midpoint of the split-capacitor and the half-bridge as the path for diverting the pulsating power.

### B. Steady-state analysis

Assume that a linear load is employed and the AC source voltage and current in single-phase converter are expressed as:

$$\begin{cases} v_s = V_s \cos \omega t \\ i_s = I_s \cos\left(\omega t + \phi\right) \end{cases} \tag{1}$$

where $V_s$ and $I_s$ are the amplitudes of AC source voltage and current, respectively. $\omega$ is the source angular frequency, $\phi$ is the displacement angle. Instantaneous power processed by the converter at the AC side can be expressed as:

$$\begin{aligned} &p\left(t\right) = u_s i_s - L\frac{di_s}{dt} i_s \\ &= \underbrace{\frac{V_s I_s}{2}\cos\phi}_{P_{dc}} + \underbrace{\frac{V_s I_s}{2}\cos\left(2\omega t + \phi\right) + \frac{\omega L I_s^2}{2}\sin\left(2\omega t + 2\phi\right)}_{\tilde{p}(t)=P\sin(2\omega t+\alpha)} \end{aligned} \tag{2}$$

where $P$ is the amplitude of double frequency ripple power, $\alpha$ is the displacement angles.

Since inductor $L_x$ is small, its stored energy can be ignored. To absorb the ripple power, the voltages across two capacitors should satisfy:

$$\frac{1}{2}C_1\frac{du_{dc1}^2}{dt} + \frac{1}{2}C_2\frac{du_{dc2}^2}{dt} = \tilde{p}\left(t\right) \tag{3}$$

where $u_{dc1}$ and $u_{dc2}$ are the voltages across the capacitors $C_1$ and $C_2$, respectively. Because the capacitance may drift by $\pm 10\%$ from its nominal value in practice, the capacitances of $C_1$ and $C_2$ are denoted as:

$$C_1 = C; C_2 = mC \tag{4}$$

where $m$ represents the unequal factor.

Substituting (2) and (4) into (3) and integrating both sides with respect to time, a quadratic equation can be obtained. Then, the steady-state voltages of the output capacitors can be solved by solving the quadratic equation, as follow:

$$\begin{cases} u_{dc1} = \frac{m u_{dc}}{1+m} \mp \frac{\sqrt{(1+m)\left(Q - \frac{P}{C\omega}\right) - m u_{dc}^2 + \frac{2(1+m)P}{C\omega}\sin^2\left(\omega t + \frac{\alpha}{2}\right)}}{1+m} \\ u_{dc2} = \frac{u_{dc}}{1+m} \pm \frac{\sqrt{(1+m)\left(Q - \frac{P}{C\omega}\right) - m u_{dc}^2 + \frac{2(1+m)P}{C\omega}\sin^2\left(\omega t + \frac{\alpha}{2}\right)}}{1+m} \end{cases} \tag{5}$$

where $Q$ is a constant, and $u_{dc} = u_{dc1} + u_{dc2}$ is the total DC-link voltage. Clearly, the capacitor voltages have an infinite number of steady-state solutions, which are characterized by superimposing the AC component on the DC component. At first sight, $u_{dc1}$ and $u_{dc2}$ are periodic functions with a period of $\pi/\omega$.

To make $u_{dc1}$, $u_{dc2}$ are the real numbers greater than zero, the constant $Q$ has to satisfy:

$$\frac{P}{C\omega} + \frac{m u_{dc}^2}{1+m} \le Q \le \frac{P}{C\omega} + \frac{u_{dc}^2}{1+m}\left(m + \min\left\{1, m^2\right\}\right) \tag{6}$$

To facilitate the selection of capacitors, we hope $C_1$ and $C_2$ have similar voltage stress. Thus, $Q$ is selected as:

$$-m u_{dc}^2 + (1+m)\left(Q - \frac{P}{C\omega}\right) = 0 \tag{7}$$

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Substituting (7) into (5) yields:

$$\begin{cases} u_{dc1} = \frac{mu_{dc}}{1+m} \mp \sqrt{\frac{2P}{(1+m)C\omega}} \sin\left(\omega t + \frac{\alpha}{2}\right) \\ u_{dc2} = \frac{u_{dc}}{1+m} \pm \sqrt{\frac{2P}{(1+m)C\omega}} \sin\left(\omega t + \frac{\alpha}{2}\right) \end{cases} \tag{8a}$$

$$\begin{cases} u_{dc1} = \frac{mu_{dc}}{1+m} \mp \sqrt{\frac{2P}{(1+m)C\omega}} \left|\sin\left(\omega t + \frac{\alpha}{2}\right)\right| \\ u_{dc2} = \frac{u_{dc}}{1+m} \pm \sqrt{\frac{2P}{(1+m)C\omega}} \left|\sin\left(\omega t + \frac{\alpha}{2}\right)\right| \end{cases} \tag{8b}$$

As can be seen from (8a), the AC component of the capacitor voltages is a sine waveform with the fundamental frequency of the AC source voltage. While the solutions in (8b) contain an amount of harmonics, which are multiple of the fundamental frequency of $2\omega$. They both have relatively close voltage stresses of split-capacitors, but the solution in (8b) is more difficult to control. Hence, we focus on the special solution shown in (8a).

### C. Average Model

According to Fig. 1, the state-space average model of the converter is expressed as follows:

$$L\frac{di_s}{dt} = v_s - d_{ab}\left(u_{dc1} + u_{dc2}\right) \tag{9}$$

$$L_x\frac{di_x}{dt} = d_x u_{dc1} - \left(1 - d_x\right) u_{dc2} \tag{10}$$

$$C\frac{du_{dc1}}{dt} = d_{ab} i_s - d_x i_x - i_o \tag{11}$$

$$mC\frac{du_{dc2}}{dt} = d_{ab} i_s + \left(1 - d_x\right) i_x - i_o \tag{12}$$

where $d_{ab}$ is the modulation signal applied to the full-bridge (positive logic to $S_1$), $d_x$ is the duty cycle of the switch $S_5$ during each switching cycle, $i_x$ is the current through the filtering inductor $L_x$, $i_o$ is the DC-link load current, and $v_s$, $i_s$ are the input voltage and current respectively.

Define the control input variable as $\xi = [1-(1+m)\,d_x]\,u_{dc}$ and capacitor voltage error as $u_\Delta = u_{dc1} - mu_{dc2}$, then (10) can be rewritten as (13). And the capacitor voltage error dynamic equation can be obtained by subtracting (12) from (11). For simplicity, assuming that the AC source current has been well regulated and the load is a resistor ($R_L$), then $i_s d_{ab} u_{dc} = p(t)$ and $i_o u_{dc} = u_{dc}^2/R_L$. Combining (11) and (12), (15) is obtained.

$$(1+m)\,L_x\frac{di_x}{dt} = u_\Delta - \xi \tag{13}$$

$$C\frac{du_\Delta}{dt} = -i_x \tag{14}$$

$$mC\frac{du_{dc}^2}{dt} = 2\left(m+1\right)\left(p(t) - \frac{u_{dc}^2}{R_L}\right) + 2\xi i_x \tag{15}$$

## III. Controller Design and Analysis

There are four control targets for the single-phase converter with DC-split-capacitor circuit:

1) to obtain the desired sinusoidal grid currents;
2) to regulate the DC-link voltage;
3) to maintain balanced capacitor voltage in average sense;
4) to minimize the DC-link ripple voltage.

To achieve the above targets, the developed rectification control and adaptive power decoupling control method are illustrated in Fig. 2.

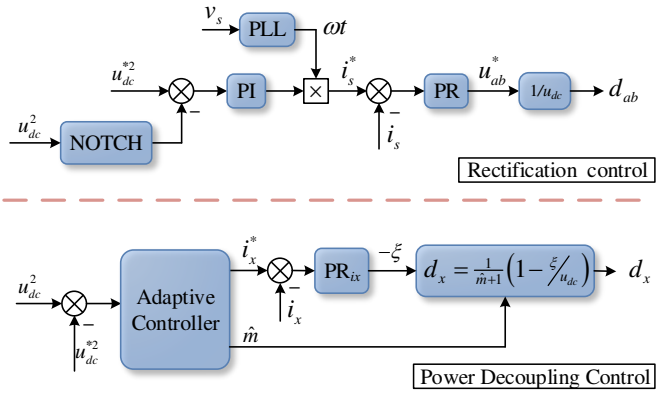


Fig. 2. Proposed control diagram for single-phase power converter with DC-split-capacitor power decoupling circuit.

### A. Controller design for Rectifier

Typically, the rectifier circuit and the decoupling circuit are independently and separately controlled [15]–[17]. For the rectifier, the control block diagram is shown in the upper part of Fig. 2. As seen, a notch filter is employed to eliminate the effect of harmonics in DC-link voltage. To realize zero steady-state error of the AC source current, a proportional-resonant (PR) controller is used.

### B. Controller design for power decoupling circuit

*1) Control scheme for filter inductor current:* For realizing the power decoupling scheme in the form of (8a), the filter inductor current $i_x$ is controlled to be a sine wave with the source frequency. Then, a PR controller with resonant peaks at $\omega$, as shown in (16), is designed as follows.

$$PR_{ix}\left(s\right) = k_{pix} + k_{rix}\frac{s}{s^2+\omega^2} \tag{16}$$

where $k_{pix}$ and $k_{rix}$ are the controller gains. The corresponding current control block diagram is shown in the lower part of Fig. 2. The current reference $i_x{}^*$ is obtained by an adaptive controller, which will be introduced in the following section.

*2) Adaptive power decoupling control:* Define an error as $\Delta x = u_{dc}^2 - u_{dc}^{*2}$, then (15) can be rewritten as:

$$mC\frac{d\Delta x}{dt} = 2\left(m+1\right)\tilde{p}(t) - 2\left(m+1\right)\frac{\Delta x}{R_L} + 2\xi i_x \tag{17}$$

As seen from (17), if $\xi i_x$ is regarded as the control input, it seems that it is easy to design a control law. However, it is

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not the case because $i_x$ has zero-crossing points in its steady-state trajectory, which leads to singularity. In this paper, an adaptive power decoupling controller is designed to avoid this singularity.

It is reasonable to assume that the ripple power is periodic with a known frequency. Let

$$2C\left(m+1\right)\tilde{p}(t)=A\cos 2\omega t+B\sin 2\omega t \tag{18}$$

where unknown constants $A$ and $B$ are related to the ripple power amplitude $P$, capacitance $C$, unequal factor $m$, and angle $\alpha$.

In this paper, $A$ and $B$ are estimated online, and a suitable current reference is constructed accordingly to achieve power decoupling. And the block diagram of the proposed adaptive controller is shown in Fig. 3. Therein, the adaptive controller output $i_x^*$ is constructed as follows:

$${i_x}^*=-\sigma\omega\cos\left(\omega t+\varphi\right) \tag{19}$$

where intermediate parameters $\sigma$ and $\varphi$ are obtained as follow:

$$\begin{cases}\sigma=\sqrt{\frac{1}{\omega}\sqrt{\hat{A}^2+\hat{B}^2}}\\ \varphi=\frac{1}{2}\arctan\left(\hat{A}\Big/\hat{B}\right)\end{cases} \tag{20}$$

And the adaptive laws are designed as:

$$\dot{\hat{A}}=k_A\Delta x\cos 2\omega t \tag{21}$$

$$\dot{\hat{B}}=k_B\Delta x\sin 2\omega t \tag{22}$$

$$\dot{\hat{m}}=-\frac{2k_m}{\hat{m}+1}u_{dc}i_x\Delta x \tag{23}$$

where $k_A$, $k_B$, and $k_m$ are positive real constants, called parameter adaptation gain. And $\hat{m}$ is the estimated value of $m$.

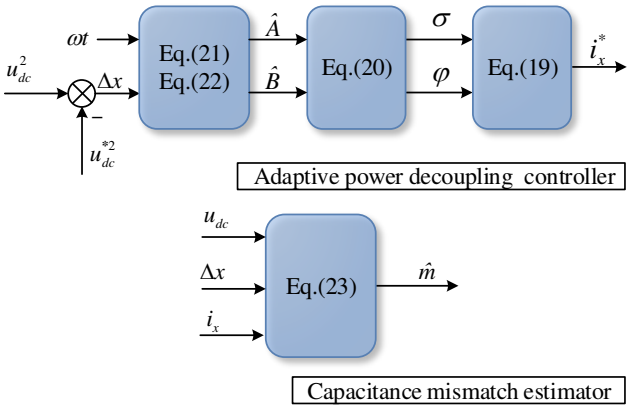


Fig. 3. The diagram of the proposed power decoupling controller.

Next, the Lyapunov stability of the proposed adaptive controller will be proved in the following.

Since the unequal factor $m$ is unknown, the duty cycle $d_x$ is obtained by $\xi=[1-(\hat{m}+1)d_x]u_{dc}$. As a result, the relationship between the actual control input $\xi_{real}$ and the control input $\xi$ is:

$$\xi_{real}=\frac{m+1}{\hat{m}+1}\xi-\frac{m-\hat{m}}{\hat{m}+1}u_{dc} \tag{24}$$

Supposing that the filtering inductance $L_x$ is small enough, then $\xi_{real}=u_\Delta$ is obtained by volt second balance. Assuming that the current $i_x$ has been tracked perfectly by the PR controller. Accordingly, $\xi_{real}$ can be yielded from (14) as:

$$\xi_{real}=-\frac{1}{C}\int\left({i_x}^*-\Delta i_x\right)dt=\frac{\sigma}{C}\sin\left(\omega t+\varphi\right)+D \tag{25}$$

where $D$ is the DC component of $\xi_{real}$.

As seen in (24), the DC component of $\xi_{real}$ is mainly related to the second term of (24) when the current $i_x$ has been tracked perfectly. Hence, $\xi_{real}$ can be expressed approximately as:

$$\xi_{real}\approx\frac{\sigma}{C}\sin\left(\omega t+\varphi\right)-\frac{m-\hat{m}}{\hat{m}+1}u_{dc} \tag{26}$$

Considering that the proposed adaptive controller is much slower than the filter inductor current controller. Thus, the current $i_x$ is approximately equal ${i_x}^*$on slow time scale. Consequently, substituting (19) and (26) into (17), the differential equation of the ripple error $\Delta x$ is rewritten as:

$$\begin{aligned}mC\frac{d\Delta x}{dt}=&2\left(m+1\right)\tilde{p}(t)-\frac{\omega\sigma^2}{C}\sin\left(2\omega t+2\varphi\right)\\&-2\left(m+1\right)\frac{\Delta x}{R_L}-2\frac{m-\hat{m}}{\hat{m}+1}u_{dc}i_x\end{aligned} \tag{27}$$

Following the adaptive controller, the estimation errors are selected as:

$$\begin{cases}\tilde{A}=A-\hat{A}\\ \tilde{B}=B-\hat{B}\\ \tilde{m}=m-\hat{m}\end{cases} \tag{28}$$

To prove the stability of the proposed control law, the Lyapunov function is considered as follows:

$$V=\frac{1}{2}\left(mC^2\Delta x^2+\frac{1}{k_A}\tilde{A}^2+\frac{1}{k_B}\tilde{B}^2+\frac{C}{k_m}\tilde{m}^2\right) \tag{29}$$

After some algebraic manipulations, time derivation of $V$ is derived as:

$$\begin{aligned}\dot{V}=&mC^2\Delta x\Delta\dot{x}+\frac{1}{k_A}\tilde{A}\dot{\tilde{A}}+\frac{1}{k_B}\tilde{B}\dot{\tilde{B}}+\frac{C}{k_m}\tilde{m}\dot{\tilde{m}}\\=&\tilde{A}\left(\Delta x\cos 2\omega t+\frac{1}{k_A}\dot{\tilde{A}}\right)+\tilde{B}\left(\Delta x\sin 2\omega t+\frac{1}{k_B}\dot{\tilde{B}}\right)\\&+\frac{\tilde{m}C}{\hat{m}+1}\left[\frac{\hat{m}+1}{k_m}\dot{\tilde{m}}-2u_{dc}i_x\Delta x\right]-\frac{2(m+1)C}{R_L}\Delta x^2\end{aligned} \tag{30}$$

Substituting (21)-(23) into (30) yields

$$\dot{V}=-\frac{2(m+1)C}{R_L}\Delta x^2\le 0 \tag{31}$$

As seen, the time derivation of $V$ is less than or equal to zero. Therefore, the Lyapunov stability can be guaranteed, and the tracking error $\Delta x$ will converge to zero when time tends to infinity.

TABLE I
COMPARISONS WITH THE EXISTING CONTROL METHODS

| Comparison Category | Dual Voltage Control [15] | Robust Power Decoupling Control [19] | Adaptive Neural Filter based Control [20] | Proposed |
|---|---|---|---|---|
| Current quality | Good | Good | Good | Good |
| Decoupling ability | Good | Improved | Improved | Improved |
| Capacitor voltage ripple frequency | 50 Hz | 100 Hz | 100 Hz | 50 Hz |
| Capacitance mismatch robustness | No | Yes | Yes | Yes |
| Unequal Factor estimator | No | No | No | Yes |
| Non-ideal Grid adaptability | No | No | Yes | No |
| Self-balance Analysis | None | None | None | Yes |

### C. Self-balance Analysis of Average Voltage

Assume that DC voltage has been well regulated and estimation errors are eliminated. Then the subsystem of (13)-(14) and (16) can be extended as:

$$\Lambda\frac{d}{dt}\begin{bmatrix} i_x \\ x_1 \\ x_2 \\ u_\Delta \end{bmatrix} = \underbrace{\begin{bmatrix} -k_{pix}\,(\hat{m}+1) & -k_{rix} & 0 & \hat{m}+1 \\ k_{rix} & 0 & -k_{rix} & 0 \\ 0 & k_{rix} & 0 & 0 \\ -(\hat{m}+1) & 0 & 0 & 0 \end{bmatrix}}_{A_z}\begin{bmatrix} i_x \\ x_1 \\ x_2 \\ u_\Delta \end{bmatrix} + \begin{bmatrix} u_{ex} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{32}$$

where $\Lambda = diag\left\{(\hat{m}+1)L_x \;\; k_{rix} \;\; k_{rix}/\omega^2 \;\; C(\hat{m}+1)\right\}$, $x_1$ and $x_2$ are the extended state values due to the PR controller, and $u_{ex}$ is external excitation and expressed as follow:

$$u_{ex} = k_{pix}{i_x}^* + k_{rix}\mathcal{L}^{-1}\left[\frac{s}{s^2+\omega^2}{i_x}^*\right] \tag{33}$$

To verify the self-balancing of the average capacitor voltage, the average theory [21] is considered. It is easy to know that the external excitation $u_{ex}$ is a $T$-periodic function in $t$. Thus the related "averaged system" of (32) can be derived as:

$$\frac{d}{dt}\begin{bmatrix} i_x \\ x_1 \\ x_2 \\ u_\Delta \end{bmatrix}_{av} = A_z\begin{bmatrix} i_x \\ x_1 \\ x_2 \\ u_\Delta \end{bmatrix}_{av} \tag{34}$$

where the variables with subscript '$av$' represent the average of the variables. When $k_{pix} > 0$ and $k_{rix} > 0$, the diagonal elements of $\Lambda$ are all greater than zero. And the system matrix $A_z$ could be decomposed into the sum of a negative semi-definite matrix and a skew-symmetric matrix. Thus, it can be concluded that the system is stable according to [22]. Furthermore, according to LaSalle's invariance principle, the averaged capacitor voltage error $u_{\Delta av}$ can converges to zero, which means that the capacitor voltages will be balanced automatically.

### D. Comparison

Table I summarizes the comparison results of the existing controllers and the proposed one. The dual voltage control in [15] realized the power decoupling with 50Hz capacitor voltage ripples. However, the effect of the capacitor parameter deviation was not considered. To deal with capacitance mismatches, a multi-resonance controller [19] and a total sliding-mode controller [20] are used to obtain the reference of filtering inductor current. Since the two methods are aimed at the solutions with 100 Hz ripple capacitor voltages, the requirement of high bandwidth current brings difficulty to controller design. Besides, there is no explanation for split-capacitors voltage self-balance in the existing literature. The proposed method not only can achieve power decoupling with 50 Hz capacitor voltage ripples but also eliminates the negative effect of capacitor mismatch by capacitance mismatch estimator. Besides, the estimated unequal factor can also be used for an auxiliary health monitoring of the split-capacitors. Moreover, the reason for the capacitor voltage self-balance has been explained.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

In the following simulations and experiments, a typical double-loop rectification control structure in the upper part of Fig. 2 is adopted. The tests are carried out in the following three cases: case I, the two capacitors $C_1 = C_2 = 330\mu F$, i.e. $m = 1$; case II, $C_1 = 330\mu F$, $C_2 = 450\mu F$, i.e. $m = 1.36$; case III, $C_1 = 450\mu F$, $C_2 = 300\mu F$, i.e. $m = 0.73$.

The numerical simulation was carried out for three cases on the MATLAB/Simulink platform. The specifications of the system are summarized in Table II. Simulation results are shown in Fig. 4. As seen, the grid current $i_s$ is sine shaped and in phase with the grid voltage $v_s$. In addition, the DC-link voltages $u_{dc}$ keeps constant at the given reference, which indicates that an excellent power decoupling control is achieved. As in (8a), the two capacitor voltages swing at the grid frequency as a result of buffering the ripple power. The simulation results manifest the correctness of the related mathematical derivation and the decoupling effect of the proposed method.

To verify the effectiveness of the proposed control strategy experimentally, a 600 W prototype has been built in the laboratory as shown in Fig. 5. High speed insulated gate bipolar transistor (IGBT) model FF200R12KT4 ($Infineon$) is used in the prototype. The controller board is mainly composed of a floating-point DSP (TMS320F28335) and a field-programmable gate array (FPGA EP2C8J144C8N). DSP is used to accomplish the control process and output the duty ratios, $d_{ab}$ and $d_x$, to FPGA. And the FPGA is used to generate switching driving signals of $S_1$ $S_6$.

In the following experiments, the split-capacitor is composed of two rated tolerance of 20% capacitors ($330\mu F$). And a $120\mu F$ capacitor (the actual value is $117\mu F$) is used in parallel for emulating a capacitance mismatch. Measured by Precision LCR Meter (TH2827C, $Tonghui$), the capacitances of the two capacitors in Case I are $C_1 = 301.4\mu F$ and

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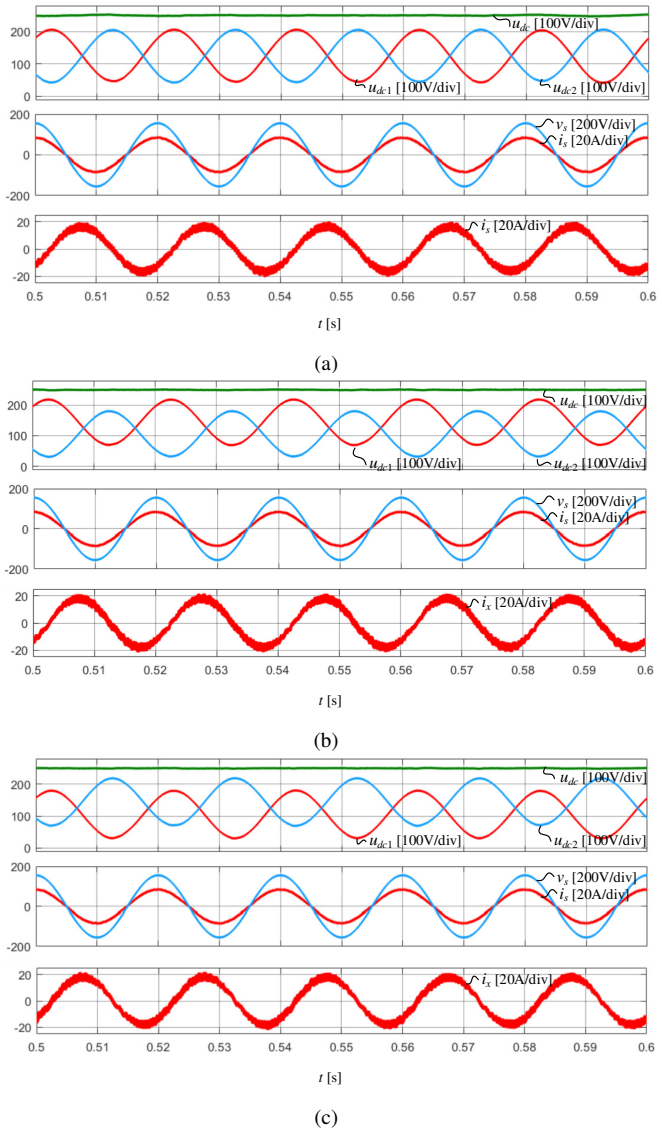


Fig. 4. Simulation results of the proposed adaptive decoupling controller. (a) Case I; (b) Case II; (c) Case III.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SETUP

| Symbol | Description | Value |
|---|---|---|
| $v_s$ | Input voltage | 110 V(rms) |
| $\omega$ | Input angular frequency | 314 rad/s |
| $L$ | Boost inductance | 3.0 mH |
| $L_x$ | filter inductance | 0.5 mH |
| $u_{dc}^*$ | DC-link voltage reference | 250 V |
| $C$ | DC-link capacitance | 330 $\mu$F |
| $R$ | DC load | 110 $\Omega$ |
| $T_s$ | Modulation period | 50 $\mu$s |
| $\omega_n$ | Natural frequency of notch filter | 100 Hz |
| $k_p, k_r$ | PR parameter | -21.4, -18950 |
| $k_{pix}, k_{rix}$ | PR parameter | -6, -400 |
| $k_A, k_B$ | Parameter adaptation gain | 0.03 |
| $k_m$ | Parameter adaptation gain | $5\times10^{-7}$ |
| $t_d$ | Dead-time | 1.0 $\mu$s |

$C_2 = 315.7\mu F$ respectively. Correspondingly, the actual values of unequal factor $m$ are listed in Table III.

In case I, since the capacitances of $C_1$ and $C_2$ are not the same actually, the capacitance mismatch estimator is enabled when the proposed decoupling controller starts up.

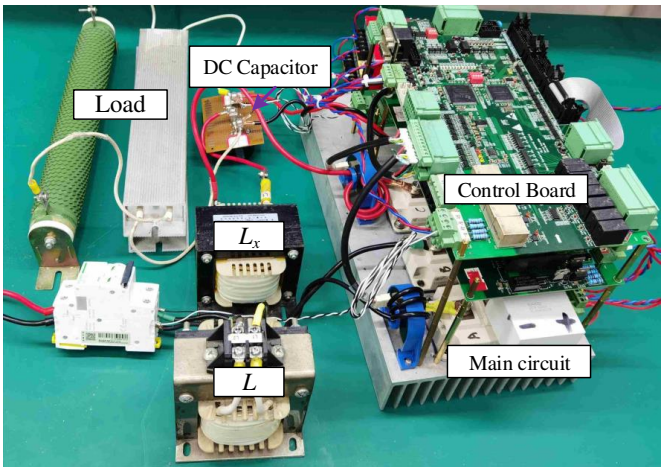


Fig. 5. Photo of the laboratory prototype.

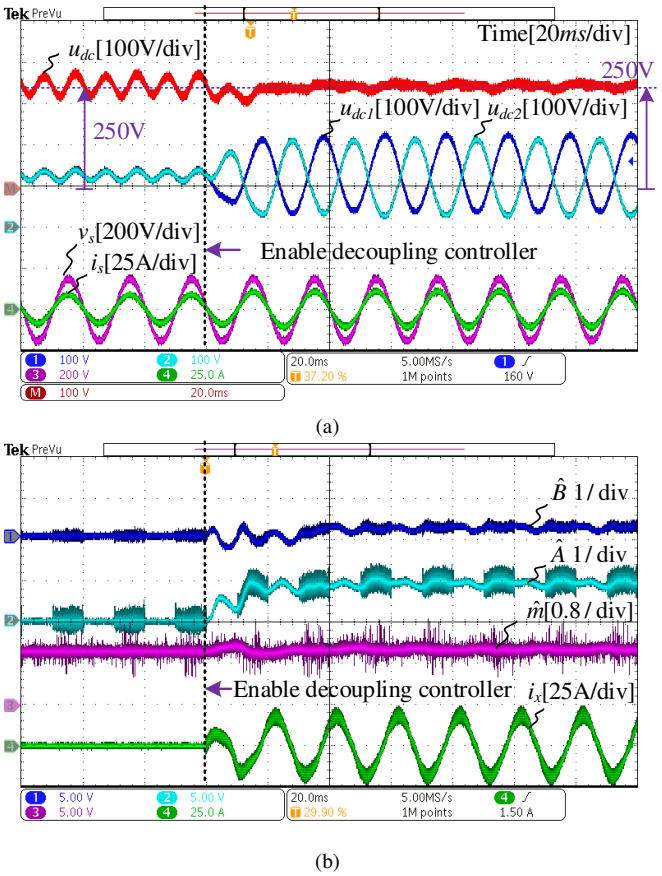


Fig. 6. Experimental results of the decoupling controller start-up in Case I (with capacitance mismatch estimator). (a) Waveforms of capacitor voltages $u_{dc1}$ and $u_{dc2}$, DC-link voltage $u_{dc}$, the input voltage $v_s$ and current $i_s$; (b) Waveforms of the estimated values of $A$, $B$, and $m$, the inductor current $i_x$.

Fig. 6 shows the experimental waveforms of the two capacitor voltages $u_{dc1}$ and $u_{dc2}$, the DC-link voltage $u_{dc}$, the input AC voltage $v_s$ and current $i_s$; while the estimated waveforms of $A$, $B$, and $m$ are shown in Fig. 6 (b). As seen, the input voltage and current are always sinusoidal and in phase with each other, which confirms the condition of unity input power factor. And the THD of the input current $i_s$ is 3.8%. Besides, there are two out-of-phase sinusoidal components in the $u_{dc1}$

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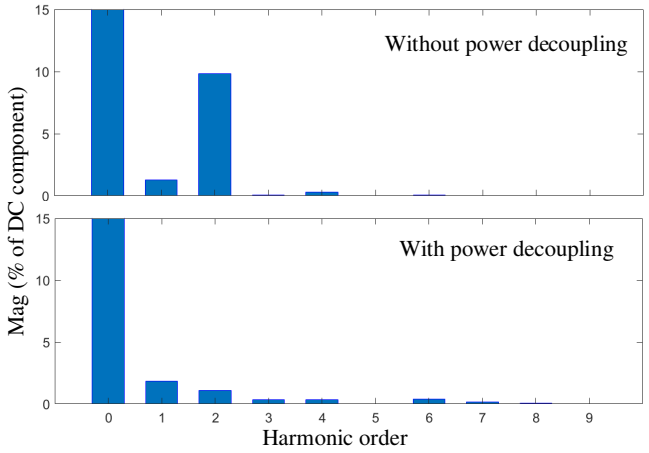


Fig. 7. The harmonic spectrum of the DC-link voltage in Case I.

and $u_{dc2}$, after the decoupling controller starts up. The DC link voltage will drop for a moment after enabling the decoupling controller. The reason is that part of the capacitor energy would be stored as a differential voltage, which will absorb certain active power when decoupling control starts up. And the AC components of the capacitor voltages also correspond to the steady-state expressions in (8a). The measured efficiencies with or without decoupling circuit are 78% and 85% respectively. This issue can be mitigated by using wide-bandgap (WBG) semiconductor devices like silicon carbide (SiC) and gallium nitride (GaN).

Besides, the frequency spectral analysis results of the DC-link voltage is shown in Fig. 7, where the interval of the frequency spectrum is 50 Hz. As seen, the second harmonic in DC-link has been reduced greatly. Correspondingly, the DC-link voltage ripple decreases from 55 V to 9 V in Fig. 6 (a). The experimental result is in good agreement with the simulated one. Thus, it can verify that the proposed adaptive controller achieves excellent power decoupling performance.

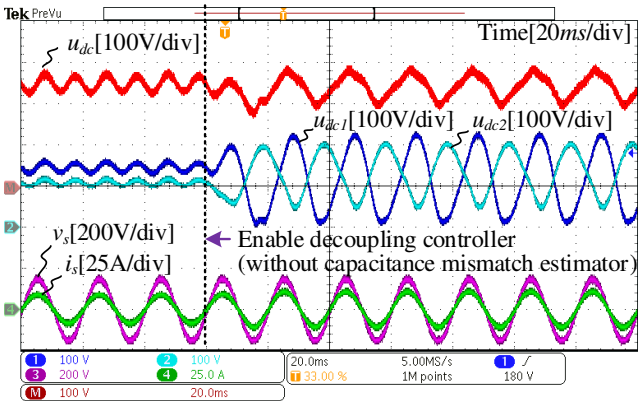


Fig. 8. Experimental results of the decoupling controller start-up in Case II (without capacitance mismatch estimator).

In case II, the capacitance mismatch of $C_1$ and $C_2$ is considered, and $m = 1.36$. According to (27), the capacitor mismatch will introduce a 50 Hz voltage ripple to the DC-link. To reduce the influence on the rectifier control, a 50 Hz notch filter is cascaded on the original 100 Hz notch filter. For comparisons, Fig. 8 and Fig. 9 (a) show the related experimental results without and with the capacitance mismatch estimator, respectively. And the corresponding harmonic spectrum of the DC-link voltage is shown in Fig. 10. From Fig. 8, the 100 Hz ripple of $u_{dc}$ is reduced with the function of the decoupling controller. However, an additional 50 Hz harmonic emerges in the DC-link voltage spectrum, which is shown in Fig. 10. Adopting the capacitance mismatch estimator, as anticipated, the undesirable 50 Hz harmonic component of the DC-link voltage is significantly attenuated in Fig. 9 (a) and Fig. 10. Thus, it is found that the converter with capacitance mismatch can also operate well under the proposed decoupling controller. Moreover, Fig. 9 (b) shows the estimated waveforms of $A$, $B$, and, $m$ in case II. As seen in Fig. 9 (b), the proposed estimator can estimate the capacitance unbalance factor in about 20 ms. Compared with Fig. 6 (b), the estimated values of $A$ and $B$ have slightly increased, which is in line with the definition of (18).

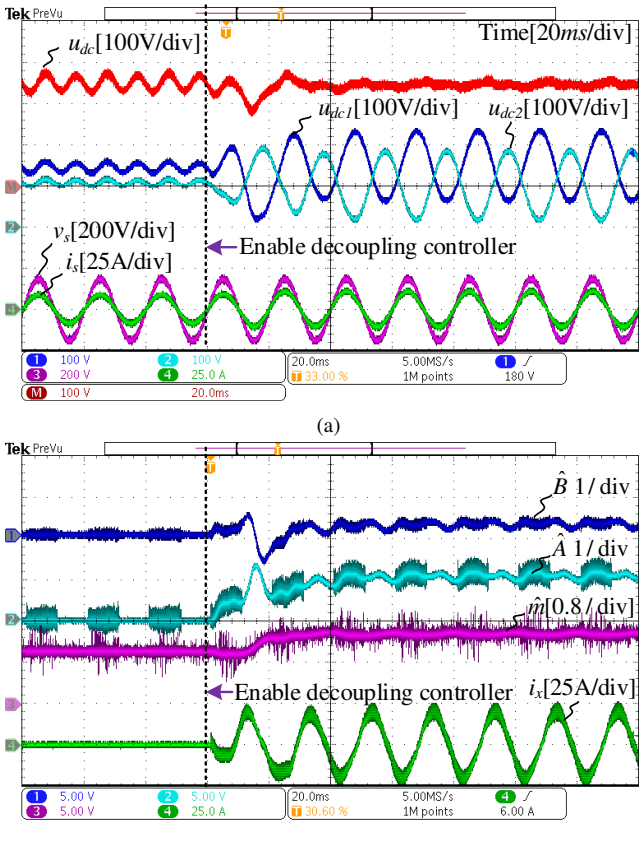


Fig. 9. Experimental results of the decoupling controller start-up in case II (with capacitance mismatch estimator). (a) Waveforms of capacitor voltages $u_{dc1}$ and $u_{dc2}$, DC-link voltage $u_{dc}$, the input voltage $v_s$ and current $i_s$; (b) Waveforms of the estimated values of $A$, $B$, and $m$, the inductor current $i_x$.

In addition, case III is performed, and Fig. 11 shows the related experimental results under the proposed decoupling control scheme. As seen, same with Case II, 50 Hz and 100 Hz harmonics of the DC-link voltage also decreases significantly. From the results in the three cases, it is found that the rectifier can still operate well regardless of the capacitance match or mismatch of $C_1$ and $C_2$, under the proposed decoupling

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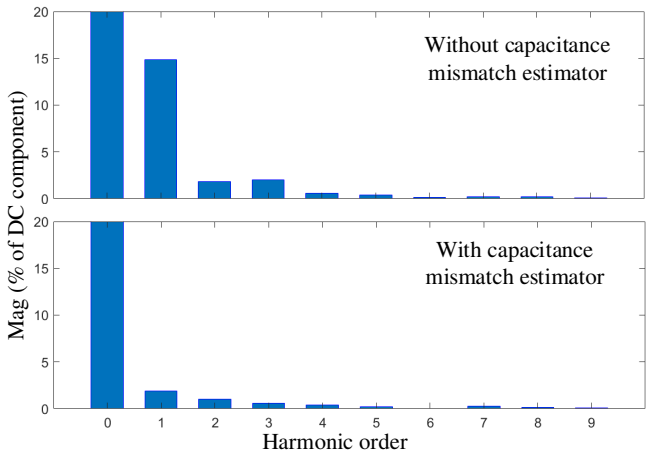
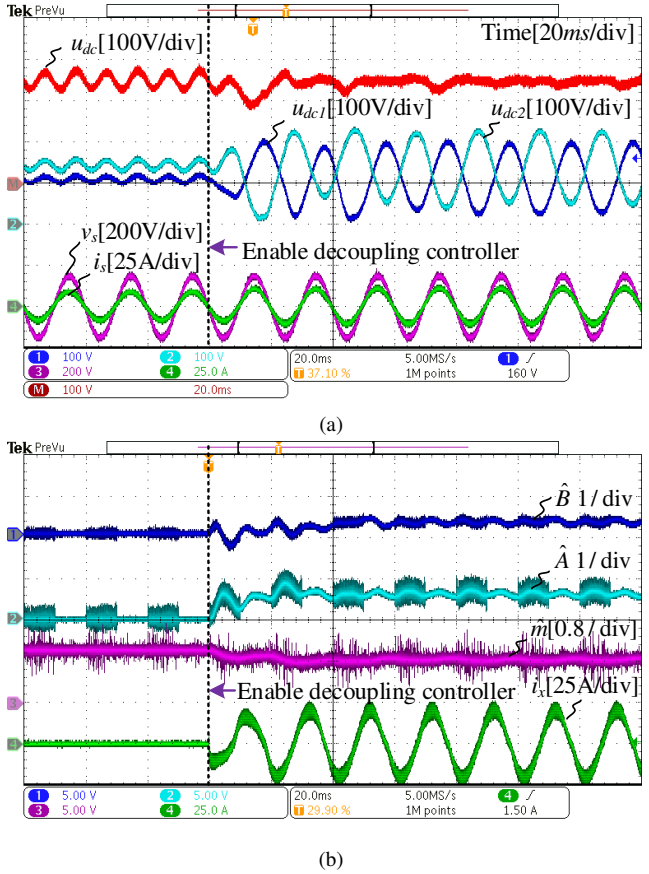



Fig. 10. The harmonic spectrum of the DC-link voltage in Case II.




(a)

(b)

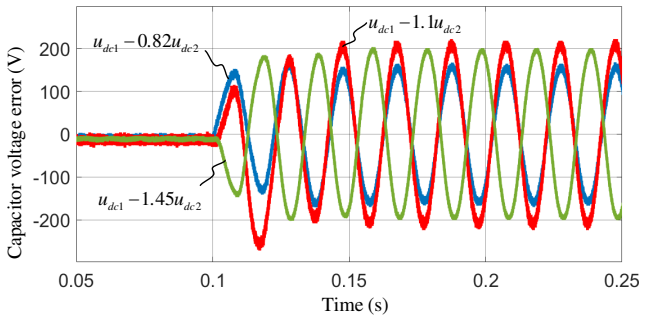
Fig. 11. Experimental results of the decoupling controller start-up in Case III (with capacitance mismatch estimator). (a) Waveforms of capacitor voltages $u_{dc1}$ and $u_{dc2}$, DC-link voltage $u_{dc}$, the input voltage $v_s$ and current $i_s$; (b) Waveforms of the estimated values of $A$, $B$, and $m$, the inductor current $i_x$.

control scheme.

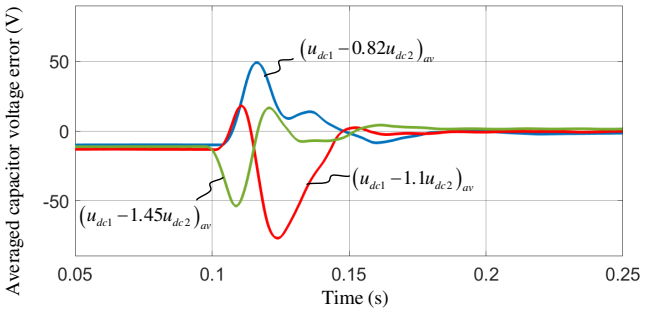
Furthermore, the estimated values and nominal values of $m$ are listed in Table III. As observed, the capacitance unequal factor is obtained online. And the unequal factor can be used as an auxiliary criterion for split-capacitors health monitoring because it can reflect the health condition differences between the two split capacitors. In the health monitoring process, to determine the threshold of a fault in unequal factor estimation errors and capacitors tolerance values should be considered simultaneously. Taking capacitors with a $\pm 10\%$ tolerance as an example, if the maximum estimation error is $6\%$, and a margin of $4\%$ is considered, the upper and lower fault thresholds could be set to $1.5$ and $0.67$, respectively. It is noted that the unequal factor m can only reflect the capacitance difference, rather than determining the faults in capacitors directly. Therefore, it is only used as an auxiliary indicator for fault detection. In actual split-capacitors fault monitoring, the capacitance mismatch estimator can be combined with the equivalent capacitance and the equivalent series resistance (ESR) measurement method for fault detection [23], [24].

TABLE III
RESULTS OF CAPACITANCE MISMATCH ESTIMATOR

| Unequal Factor $m$ | Actual Value | Estimated Value |
|---|---|---|
| 0.73 | 0.754 | 0.82 |
| 1 | 1.047 | 1.1 |
| 1.36 | 1.435 | 1.45 |




(a)




(b)

Fig. 12. Waveforms of calculated variables. (a) Waveforms of the capacitor voltage error $u_\Delta$; (b) Waveforms of the capacitor averaged voltage error $u_{\Delta av}$.

To verify that the self-balance of the average capacitor voltage, the above experimental data are imported into MATLAB for analysis. By calculating capacitor voltage error $u_\Delta$ and importing into the mean block, the waveforms of $u_\Delta$ and $u_{\Delta av}$ are plotted in Fig. 12. Wherein, the estimation values in Table III are used in the calculation of $u_\Delta = u_{dc1} - m u_{dc2}$, and the fundamental frequency of the mean block is set to 50 Hz. The voltage error $u_\Delta$ has a 50 Hz oscillation excitation response with the sinusoidal in Fig. 12 (a). And the oscillation will not diverge, which corresponds to stability analysis of the system. As seen in Fig. 12 (b), the averaged error $u_{\Delta av}$ decayed to near zero. Hence, it is found that the capacitor voltage is self-balanced under the proposed scheme. It means

that the voltage sharing resistor and the voltage sensor can be eliminated in actual implementation

## V. Conclusion

In this paper, an adaptive power decoupling controller is proposed for the DC split-capacitor decoupling circuit under capacitance mismatch. The conclusions are listed below:

1) The steady-state analysis of DC split-capacitor decoupling circuits shows that there are infinite feasible solutions to achieve the decoupling of twice ripple power under capacitance mismatch. Among them, a special solution is to control the capacitor voltages into DC and the fundamental frequency sinusoidal AC component.
2) Under the framework of the special solution, an adaptive power decoupling controller is proposed to realize the decoupling of twice ripple power.
3) The capacitance mismatch estimator is presented to estimate the unequal factor online. Consequently, the fundamental frequency power ripple caused by capacitor mismatch is eliminated. Meanwhile, the estimated unequal factor can be used as a health monitoring indicator of split-capacitors.

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